Simulation of FPGA based Analog Transmission Link

FPGAs are used in a lot of applications involving data transfer and acquisition. Most of data links currently being used are of serial in nature and involve development of synchronization and clock recovery modules. The clock information is generally embedded in data itself and receiver extracts this information for decoding the link. Analog signals can be interfaced with digital world using ADC modules and after applying digital algorithms the signal can be ported to analog world using DACs.

In this project student has to learn basic concepts of FPGA and VHDL/Verilog programming and develop interfaces for ADC and DAC modules with FPGA.

The project consists of design and development of HDL codes for various functions which are required to develop such data transmission link. The student has to solve the synchronization challenges of simultaneous ADC and DAC conversion of data (upto 1 MSPS) without transmitting the clock.

The student has to develop a simulation of entire link using ModelSim , ISE (Student Edition) and report the results

Online Mode of project: Due to present pandemic the students have to develop a simulation of the entire link after selecting the ADC/DAC modules supporting upto 1MSPS data rate considering the actual application.

References: http://www.doe.carleton.ca/~tak/publications/01557348.pdf

Academic Project Requirements:

1) **Required No. of student(s) for academic project: ___2_____**

2) **Name of course with branch/discipline: ___B Tech (ECE)_____**

3) **Academic Project duration:**

   (a) **Total academic project duration: _____6_____ Months**

   (b) **Student's presence at IPR for academic project work: 5 Full working Days per week in online mode**

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